REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Claims 1-47 are currently pending. By way of this response, claim 1, 14, 16, 29, 31, 44 and 47 are amended.

Response to Rejection Under 35 USC § 103(a) in View of Eickemeyer and Kalla

In paragraphs 2-6 of the Office Action, the Examiner rejected claims 1, 13-16, 28-31, 43-45 under 35 USC § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,931,639 to Eickemeyer ("Eickemeyer") in view of U.S. Patent No. 7,013,400 to Kalla et al. ("Kalla"). This rejection is respectfully traversed.

Independent claim 1 as amended recites:

> A network processor, comprising:
>
> a fetch control unit, having an input coupled to receive an execution feedback signal with stall information related to a plurality of threads on a per thread basis, the fetch control unit generating an instruction fetch sequence based on the execution feedback signal; and
>
> an instruction cache, having an input coupled to an output of the fetch control unit, the instruction cache dispatching instruction data responsive to the instruction fetch sequence.

Support for the proposed claim amendment is found in the specification as filed at, for example, in page 14, paragraph [0039]. Thus, the claimed invention recites a fetch control unit that receives stall information related to a plurality of threads on a per thread basis, and generates an instruction fetch sequence based on the stall information. Advantageously, an instruction cache dispatches instruction data according to the generated instruction fetch sequence, thereby preventing pipeline stalls and increasing utilization of

the network processor. Amended independent claims 16 and 31 include limitations similar to claim 1.

Eickemeyer, among other differences, does not disclose "an execution feedback signal with stall information related to a plurality of threads on a per thread basis" and a fetch control unit that generates "an instruction fetch sequence based on the execution feedback signal." Eickemeyer discloses an apparatus for implementing a variable-partitioned queue for simultaneous multithreaded processors. See Eickemeyer, Abstract. More particularly, Eickemeyer discloses an instruction fetch address register that tracks and controls the address for an instruction cache. See Eickemeyer, 3:15-18. The Examiner acknowledged that Eickemeyer fails to disclose an execution feedback signal with information related to a plurality of threads on a per thread basis. See Office Action, page 2. The Examiner pointed to column 3, lines 15-37 of Eickemeyer for teaching of the fetch control unit generating an instruction fetch sequence based on the execution feedback signal. See Office Action, page 2. However, the cited section of Eickemeyer only discloses that "address tracking and control to the instruction cache 202 is provided by an instruction fetch address register 206 having one or more addresses per thread." It is all-together silent as to generating an instruction fetch sequence based on an execution feedback signal.

Kalla also fails to disclose the claim limitations cited above. Kalla discloses a method to select instructions from instruction queues for two threads using a variable counter. See Kalla, Summary. The Examiner pointed to column 6, lines 45-59 of Kalla for teaching of the "execution feedback signal with stall information related to a plurality of threads on a per thread basis." However, the cited section of Kalla only discloses forwarding information from a completion unit to an instruction fetch unit. See Kalla, 6:52-

53. It does not teach or suggest that the information relates to a plurality of threads on a per thread basis, or that the information includes stall information. Kalla is all-together silent as to the fetch control unit that generates "an instruction fetch sequence based on the execution feedback signal." Therefore, Kalla fails to at least disclose these claim limitations of amended independent claims 1, 16 and 31.

In view of the above, Eickemeyer and Kalla, whether considered singly or in combination, fail to disclose each and every limitation recited in amended independent claims 1, 16 and 31. Thus, amended independent claims 1, 16 and 31 are patentable over Eickemeyer and Kalla. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of the § 103 rejections is respectfully requested.

Response to Rejection Under 35 USC 103(a) in View of Eickemeyer, Kalla and Boggs

In paragraphs 6-9 of the Office Action, the Examiner rejected claims 32, 33 and 35 as being unpatentable over Eickemeyer and Kalla, and further in view of U.S. Patent No. 7,051,329 to Boggs ("Boggs"). This rejection is respectfully traversed.

Independent claim 31 as amended recites:

> A method for fetching instructions in a network processor, comprising:
>
> generating an instruction fetch sequence based on an execution feedback signal with stall information related to a plurality of threads on a per thread basis; and
>
> dispatching instruction data responsive to the instruction fetch sequence.

Dependent claims 32, 33 and 35 are dependent on independent claim 31, and thereby incorporate by reference all the limitations of claim 31.

The above arguments with respect to independent claim 1 are applicable here to establish that Eickemeyer and Kalla, whether considered singly or in combination, fail to disclose claim limitations of claim 31. Specifically, they fail to disclose "an execution feedback signal with stall information related to a plurality of threads on a per thread basis" and generating an instruction fetch sequence based on the execution feedback signal.

Boggs similarly fails. Boggs discloses a method for managing resources in a multithreaded processor. See Boggs, Abstract. More particularly, Boggs discloses a trace delivery engine that feeds back a stall signal to a microinstruction translation engine. See Boggs, Figure 2. The stall signal causes the trace delivery engine to stall until the stall conditions are cleared. See Boggs, 11:39-44. However, Boggs fails to teach or suggest "an execution feedback signal with stall information related to a plurality of threads on a per thread basis." The stall signal in Boggs is thread specific and not "related to a plurality of threads on a per thread basis." See Boggs, 11:51-63, see also Office Action dated June 28, 2006, paragraph 4 (the Examiner acknowledged that Boggs fails to disclose an execution feedback signal with information related to a plurality of threads on a per thread basis). It follows that Boggs also fails to disclose generating an instruction fetch sequence based on the execution feedback signal.

In view of the above, Eickemeyer, Kalla, and Boggs, whether considered singly or in combination, fail to disclose each and every limitation recited in amended independent claim 31. Thus, amended independent claim 31 is patentable over Eickemeyer, Kalla, and Boggs. Dependent claims 32, 33 and 35 are allowable for at least the same reasons. Accordingly, withdrawal of the § 103 rejections is respectfully requested.

In paragraph 10 of the Office Action, the Examiner indicated that claim 47 is allowed. Applicants respectfully submit that claim 47 is amended to correct spell mistake by replacing "wherien" with "wherein," and the scope of the claim remains the same.

In paragraph 11 of the Office Action, the Examiner objected to claims 2-12, 17-27, 34 and 36-42, and indicated that they are allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In view of the above, Applicants respectfully submit that these claims are allowable and request the withdrawal of the objections.

Conclusion

Applicants respectfully submit that the pending claims are allowable over the cited references, and request that the application be passed to issue. The Examiner is invited to contact the undersigned by telephone to advance the prosecution of this application.

Respectfully submitted,
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